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AMERICAN SOCIETY FOR TESTING AND MATERIALS
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Standard Test Method for Sheet Resistance Uniformity Evaluation by In-Line Four-Point Probe with the Dual-Configuration Procedure [1]

This standard is issued under the fixed designation F 1529; the number immediately following the designation indicates the year of original adoption or, in the case of revision, the year of last revision. A number in parentheses indicates the year of last reapproval. A superscript epsilon (ϵ) indicates an editorial change since the last revision or reapproval.

ϵ[1] NOTE—Table A1.2 corrected editorially and the year date was changed to Dec. 5, 1997.

INTRODUCTION

This test method uses a four-point probe in a manner different from that of other ASTM methods for the measurement of the resistivity or sheet resistance of semiconductors. In this test method, two different ways (configurations) of connecting the probe pins to the electronics that supply current and measure voltage are used at each measurement location on the specimen. This use of a four-point probe is often referred to as "dual-configuration" or as "configuration switched" measurements.

There are three benefits that result from the second measurement configuration at each location: (*1*) the probe no longer needs to be in a high symmetry orientation on the specimen, that is, being perpendicular or parallel to the radius on a circular wafer or to the length or width of a rectangular specimen, as long as it is a modest distance from the edge of the wafer, (*2*) the lateral dimension(s) of the specimen, and the exact location of the probe on the specimen no longer have to be known—the geometric scaling factor results directly f rom the two sets of electrical measurements at each location, (*3*) the two sets of measurements self-correct for the actual separations between the probe pins in a manner that has been shown to be more effective than measuring probe impressions made on a piece of polished material. As a result, high precision measurements can be made with smaller probe separations than is possible with single configuration use of a four-point probe, thus allowing higher spatial resolution of wafer sheet resistance variations. **(1)** [2]

1. Scope

1.1 This test method covers the direct measurement of the sheet resistance and its variation for all but the periphery (amounting to three probe separations) for circular conducting layers pertinent to silicon semiconductor technology. These layers may be fabricated on substrates of any diameter that is capable of being securely mounted on a prober stage.

NOTE 1—The equation used to calculate the sheet resistance data from measurements is not perfectly accurate out to the edge of the wafer for probes oriented at an arbitrary angle with respect to a wafer radius. Further, automatic instruments on which this test method will be performed may not have perfect centering of the wafer on the measurement stage. These factors require that the periphery of the layer being measured be excluded. Also, many thin film processes use wafer clamps that preclude forming layers out to the edge of the substrate. The edge exclusion in this test method applies to the film that is being measured, rather than to the substrate. The equation used is based on mathematics developed for layers of circular shape. It is expected to work well for layers of other shapes such as rectangular, if edge exclusion requirements are met; however, the accuracy near the edge of other shapes has not been demonstrated **(2).**

1.2 This test method is intended primarily for assessing the uniformity of layers formed by diffusion, epitaxy, ion implant and chemical vapor, or other deposition processes on a silicon substrate. The deposited film, which may be single crystal, polycrystalline or amorphous silicon, or a metal film, must be electrically isolated from the substrate. This can be accomplished if the layer is of opposite conductivity type from the substrate or is deposited over a dielectric layer such as silicon dioxide. This test method is capable of measuring films as thin as 0.05 μm, but particular care is required for establishing reliable measurements for most films in the range below 0.2 μm. Films that have a thickness up to half the probe separation can be measured without the use of a thickness-related correction factor. It may give misleading results for films formed by silicon on insulator technologies because of charge or charge trapping in the insulator.

1.3 This test method can be used to measure the sheet resistance uniformity of bulk substrates. However, the thickness of the substrate must be known to be constant or must be

[1] This test method is under the jurisdiction of ASTM Committee F-1 on Electronics and is the direct responsibility of Subcommittee F01.06 on Silicon Materials and Process Control.

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[2] The boldface numbers in parentheses refer to the list of references at the end of this test method.

measured at all positions where sheet resistance values are measured in order to calculate relative variations in resistance reliably.

NOTE 2—The thickness correction factor for layers that are thicker than 0.5 times the probe spacing is known to vary more rapidly than that for single-configuration four-probe measurements, but such a correction has not yet been published. Until such a correction is published, resistivity values determined by the dual-configuration method will not be accurate for these thicker specimens; however, if the wafer has uniform thickness, variations of resistivity can still be determined by this test method.

1.4 This test method can be used to measure sheet resistance values from below 10 mΩ for metal films, to over 25 000 Ω for thin silicon films. However, for films at the upper end of this resistance range, and for films toward the low end of the thickness range, the interpretation of the sheet resistance values may not be straightforward due to various semiconductor effects **(3, 4, 5)**.

NOTE 3—The principles of this test method are also applicable to other semiconductor materials, but the appropriate conditions and the expected precision have not been established.

1.5 This test method uses two different electrical configurations of the four-point probe at each measurement location. It does not require measurement of probe location on the wafer, or probe separations, or of wafer diameter (except to determine edge exclusion for measurement-site selection) as do other four-point probe methods such as Test Methods F 81, F 84 and F 374. By use of electrical data from the two different configurations at each location, the method is self-calibrating with respect to the geometrical parameters **(1)**.

1.6 This test method is intended to be used on automated wafer testing systems that use *R*-theta or *X-Y* stage positioning for the measurements. The rapid calculations for sheet resistance used in this test method are based on more extensive calculations, and are within 0.1 % of the results of those more extensive calculations, even if the probes are not oriented parallel or perpendicular to a wafer radius, providing that the probes are more than 3-probe spacings from the edge of the layer being measured **(1)**, **(2)** (see Note 1).

1.7 The values stated in SI units are to be regarded as the standard. The values given in parentheses are for information only.

1.8 *This standard does not purport to address all of the safety concerns, if any, associated with its use. It is the responsibility of the user of this standard to establish appropriate safety and health practices and determine the applicability of regulatory limitations prior to use.*

2. Referenced Documents

2.1 *ASTM Standards:*

D 1193 Specifications for Reagent Water [3]

F 42 Test Methods for Conductivity Type of Extrinsic Semiconducting Materials [4]

F 81 Test Method for Measuring Radial Resistivity Variation on Silicon Slices [4]

F 84 Test Method for Measuring Resistivity of Silicon Wafers with an In-Line Four-Point Probe [4]

F 374 Test Method for Sheet Resistance of Silicon Epitaxial, Diffused, Polysilicon, and Ion-Implanted Layers Using an In-Line Four-Point Probe [4]

F 1241 Terminology of Silicon Technology [4]

2.2 *SEMI Standards:*

SEMI C1 Specifications for Reagents [5]

3. Terminology

3.1 *Definitions:*

3.1.1 For definitions of terms used in silicon wafer technology refer to Terminology F 1241.

4. Summary of Test Method

4.1 An in-line four-point probe is used to determine the specimen sheet resistance at each desired measurement location. The number and positioning of measurement locations is determined by end-use needs, or by the parties to the test in the case of referee measurements. At each location, a direct current is passed into the specimen, using two of the probes, as specified, and the potential difference is measured using the other two probes. Current polarity is reversed and the potential difference is remeasured to allow elimination of thermoelectric effects. Before the probe is raised, the process is repeated using a different combination of probes, as specified. At each location, the sheet resistance is obtained from the four ratios of potential difference to current.

4.2 The adequacy of the probe is determined both by optical examination of probe indentations made in a polished silicon surface, and by a performance test on a wafer of the type whose uniformity is to be checked.

4.3 The accuracy of the electronics is tested by means of an analog circuit emphasizing the performance and noise immunity of the electronics in the presence of large contact resistances of the probe tips to the semiconductor surface.

5. Significance and Use

5.1 The sheet resistance of epitaxial, implanted, diffused or deposited films is an important materials acceptance and process control parameter. The uniformity across a wafer of the sheet resistance resulting from any of these processes is important for the equivalence of performance of devices or circuits made from various regions of the wafer.

5.2 This test method is suitable for use in materials acceptance, equipment qualification, process control, research, and development.

6. Interferences

6.1 Photoconductive and photovoltaic effects can seriously influence the measured sheet resistance, particularly with high resistivity layers or those with very shallow junctions. Therefore, all measurements should be made in a darkened enclosure unless experience shows that the material of interest is insensitive to ambient illumination.

6.2 Spurious currents can be induced in the test circuit when the equipment is located near high-frequency generators. If

[3] *Annual Book of ASTM Standards*, Vol 11.01.

[4] *Annual Book of ASTM Standards*, Vol 10.05.

[5] Available from Semiconductor Equipment and Materials International, 805 East Middlefield Rd, Mountain View, CA 94043.

such a location is unavoidable, adequate shielding must be provided.

6.3 Minority carrier injection during the measurement can occur due to the electric field in the specimen. With material possessing a long minority-carrier lifetime and moderate to high resistivity, such injection can result in a lowering of the resistivity (sheet resistance) for a distance of several centimetres from the point of injection. Carrier injection can be detected by repeating the measurements at lower current. In the absence of injection, no increase in resistivity should be observed at the lower current. The current level recommended, (see Table 1) should reduce the probability of difficulty from this interference to a minimum, but in cases of doubt the measurements should be repeated at a lower current level. If the proper current is being used, doubling or halving its value should result in a change of sheet resistance that is less than 0.5 %.

6.4 Semiconductors have a significant temperature coefficient of resistivity. Consequently, the measurement current used should be small to avoid resistive heating. The current levels recommended should reduce the chances of this problem. If resistive heating is suspected, it can be detected by a change in readings starting immediately after the current is applied. If such a change is observed, repeat the electrical measurements at a lower current. In the absence of Joule heating, the temperature of the water should be uniform if the wafer is mounted on a chuck having good thermal conductivity and large thermal mass. Sheet resistance maps should not be distorted by temperature nonuniformities in this case. Coefficients for the temperature variation of the sheet resistance of a particular layer type will depend upon the specific dopant, or resistivity, profile of that layer type, and must be evaluated empirically for the layer fabrication process being used if correction of data to a fixed reference temperature is desired.

6.5 Vibration of the probe may cause variations in contact resistance, which is often manifested as unstable readings. If difficulty is encountered, the apparatus should be vibration isolated.

6.6 Penetration of either the current or voltage probes through the layer being measured to the substrate will result in erroneous readings. This can usually be checked by mounting the specimen directly on a metal support that is grounded to the current supply and by then looking for a reduction in measured specimen voltage in at least one polarity as the ground connection is removed and replaced. If this condition occurs, examine the probe tips microscopically for sharp asperities and remove these by polishing or otherwise conditioning the probe tip, or else reduce the probe force or use a probe with blunter probe tips.

TABLE 1 Nominal Current Values for Measurement of Sheet Resistance

Sheet Resistance, Ω	Current [A]
2–25	10 mA
20–250	1 mA
200–2500	100 µA
2000–25 000	10 µA

[A] The current used should be from one-half to twice the nominal value and should be chosen to give a measured voltage on the specimen that is between 7 and 15 mV when using Configuration A. Once the current is selected for forward direction measurements at a given site, it must be kept constant to 0.01 % for the remaining measurements at that site.

6.7 Use of two electrical configurations at each measurement site eliminates the need for measurement of geometric separation of the probe tips in order to analyze the data. As a result, even for referee measurements, any probe spacing that is agreed upon between the parties to the test and demonstrates sufficiently low data scatter may be used for this test method.

6.8 Use of the data from the two electrical configurations to calculate a factor for water diameter and for position of the measurement site on the wafer will be accurate to within 0.1 % as long as the measurement site is away from the perimeter of the wafer. To meet this requirement the site should be at least five-probe separations from the perimeter for the case of probe alignment perpendicular to a wafer diameter, and at least three-probe separations from the perimeter for the case of probe alignment parallel to a wafer diameter. For certain processes, such as ion implantation, use of a wafer clamp during layer formation causes a p-n layer-to-substrate junction on the top surface of the wafer interior to the mechanical edge of the wafer. In these cases, the probe separation values above refer to the location of the measurement site with respect to such junctions.

6.9 In shallow or lightly-doped layers, an effect known as carrier redistribution will cause the number of free carriers in the layer to be different from the number of dopant atoms. As a result, sheet resistance values measured by this test method may be noticeably different from values calculated from models that imply the dopant and free-carrier depth profiles to be equivalent.

6.10 Surface and near-surface effects, such as the formation of hydrogen complexes with acceptors, may occur during or immediately after the fabrication of many thin films, particularly if lightly doped. They may also occur slowly with storage. These effects may be uniformly or nonuniformly distributed across the wafer surface. The result is to modify, generally by way of increasing, the measured sheet resistance. Two of the most prominent impacts of these effects are to make the results of a given process step appear to be more nonuniform than is actually the case, and to shift the absolute level of a reference wafer used to monitor the performance of the mapping tool so as to make the tool appear to be out of control.

7. Apparatus

7.1 *Specimen Preparation*:

7.1.1 *Chemical Laboratory Apparatus*, such as plastic beakers, graduated cylinders, and plastic coated tweezers for use both with acids and with solvents. Proper facilities for handling and disposing of acids and their vapors are essential.

7.1.2 *Hot Plate*, large enough to heat wafer of interest to 200°C.

7.2 *Probe Assembly*:

7.2.1 *Four-Point Probe*, having conical probe tips of a durable material such as tungsten-carbide. The included angle of the tips shall be in the nominal range 45 to 150°. The probe tips shall be in a straight line with nominally equal separations in the range 250 µm (0.010 in.) to 1590 µm (0.0625 in.). An isolation resistance between adjacent probes, a factor of 10^5 larger than the sheet resistance of the film is required; a value

of $10^{9}\Omega$, or greater, is recommended for the widest general application. Recommended tip radii and probe force values are slightly different depending upon whether the probe force is applied by springs, or deadweight, as follows:

7.2.1.1 *Spring-Loaded Probes*, should have tips that terminate in a radius in the nominal range 25 to 250 µm or in a flat circular truncation of the cone with a circle diameter in the range 50 to 125 µm. A probe force per pin of 0.25 to 2.0 N (approximately 25 to 200 gf) may be needed to cover the variety of films that are covered under the scope of this test method.

7.2.1.2 *Deadweight Loaded Probes*, should have probe tips that terminate in a radius of at least 19 µm. A probe force per pin of 0.1 to 1 N (approximately 10 to 100 gf) may be needed to cover the variety of films that are covered under the scope of this test method.

NOTE 4—In general, the blunter the probe tip, the higher the probe force that is used to make good electrical contact to the layer. Conversely, the sharper the probe tip, or the thinner the layer, the lighter the probe force that should be used. The upper end of the allowed probe force range is generally used only for buried-peak conducting layers, such as MeV implants, or for high-resistivity, thick epitaxial layers. General experience indicates that there is not a simple specification of one or two combinations of probe radius and probe force that will cover all layers of interest. Recent experience with conditioning probe tips against materials such as a sapphire or non-polished ceramic substrate, or even on a piece of lapped silicon, indicates that the microroughness of the probe tip is a very important, but not-readily specifiable parameter for the proper probe type in a given application. The combination of probe radius and force that is chosen affects both the likelihood of probe penetration and the quality of electrical contact, which in turn affects the measurement noise and accuracy. A use test is given to aid in verifying appropriateness of a given probe for a specific layer type. Controlled lowering of the probe pins so that contact is made without lateral scrubbing of the probes against the wafer surface has been found to be very important.

7.3 *Microscope*:

7.3.1 The microscope for inspecting probe damage shall have a magnification of at least 600 ×, and an eyepiece magnification no greater than 15 ×. The microscope shall be capable of dark-field, interference contrast, or oblique illumination.

7.3.2 The microscope shall have a stage capable of moving the specimen in order to examine a number of adjacent damage marks made by each of the four probe points.

7.4 *Measurement Stage*:

7.4.1 *The Stage of the Wafer Prober*, shall have a vacuum chuck or comparable means of holding the wafer securely during measurement. This vacuum chuck should be of sufficient thermal mass to keep the wafer at a constant temperature, within 1°C, during the time required for all measurements. The stage should be provided with stops, pins, engraved circles, or other means for accurately and repeatedly positioning wafers. For measurements on wafers where the deposited or fabricated film may extend over the edges of the substrate and make contact to the backside, a thin layer of mica, or other electrical insulator must be used between the wafer and the chuck.

7.4.2 *The Probe Assembly Support*, must allow the probes to be lowered onto the wafer surface with no evidence of lateral movement (probe skidding). This requirement can be verified by lowering and raising the probes a number of times onto a polished silicon surface with steps of 50 to 100 µm between these locations, and then observing the probe damage marks for each of the probe points with the required microscope.

NOTE 5—For a probe with blunt tips or well-conditioned probe points, it is generally very difficult to view the probe damage with bright field illumination; use of dark-field, Nomarski, or oblique illumination is recommended. To aid in locating the probe damage, the formation of a grid of rectangles, by scribing, etching or other suitable process on a polished wafer surface, has been found helpful. The rectangles should be large enough to allow all four-probe points to be readily located within the boundaries and a number of probe impressions to be made within the confines of a single rectangle.

7.4.3 *The Wafer Probe Stage*, shall have a sufficient range of motion to allow probing all desired locations on the largest wafers to be measured. Except for restrictions on the exclusion of three-probe spacings at the perimeter of the layer being measured, the accuracy of sheet resistance measurements using this test method do not require any particular accuracy on the position coordinates.

NOTE 6—If this test method is used for referee measurements, uncertainty in position coordinates may produce accurate measurements at the locations measured but may make comparison of data more difficult. It is recommended that the wafer be centered on the stage with an accuracy of 1 mm, or better, and that all positions measured, have coordinates controlled with an accuracy of 10 µm, or better, with respect to the center of the stage.

7.4.4 *The Wafer Stage*, shall be instrumented with a temperature monitor to be used for any application where the average sheet resistance of the layer is a parameter to be reported. The temperature monitor may be of any convenient type, but must be accurate to 0.3°C, or better.

7.5 *Electrical Measuring Apparatus*:

7.5.1 The conceptual layout of the electronic circuitry is shown in Fig. 1 for the case where a standard resistor is used to monitor the applied current. The standard resistor can be omitted if the current value is set or known directly.

7.5.1.1 *Constant DC-Current Source*—This must have sufficient compliance voltage to supply a constant current that results in a measured voltage drop on the specimen that is between 5 and 20 mV. Currents between 10^{-6} and 10^{-2} A are required if the sheet resistance range 1 to 20 000 Ω is to be covered. The output current must be stable to 0.01 %, or better, during the time required to take all data at each location; ripple and other noise must be less than 0.1 % of the d-c current level. A compliance voltage in excess of 10 V is generally not needed unless measurements must be made through a significant layer of oxide or other dielectric. A standard resistor (7.5.2) is needed to determine measurement current unless the current supply is in calibration and known to output a d-c current that is within 0.1 % or better of the set-point value. A wet or dry battery may be used for the current source providing there is means for regulating the output current.

NOTE 7—The range of specimen voltage drops given in 7.5.1.1 is an operational compromise. It is based on keeping measurement values large enough so that voltage measurements with submicrovolt resolution are not required, that the precision attainable with the dual-configuration procedure is not limited by the number of significant figures in the measurement data, and that the risk of certain errors due to semiconductor effects occurring at higher measurement currents are avoided. However, for certain applications of interest, such as metal films and very heavily doped

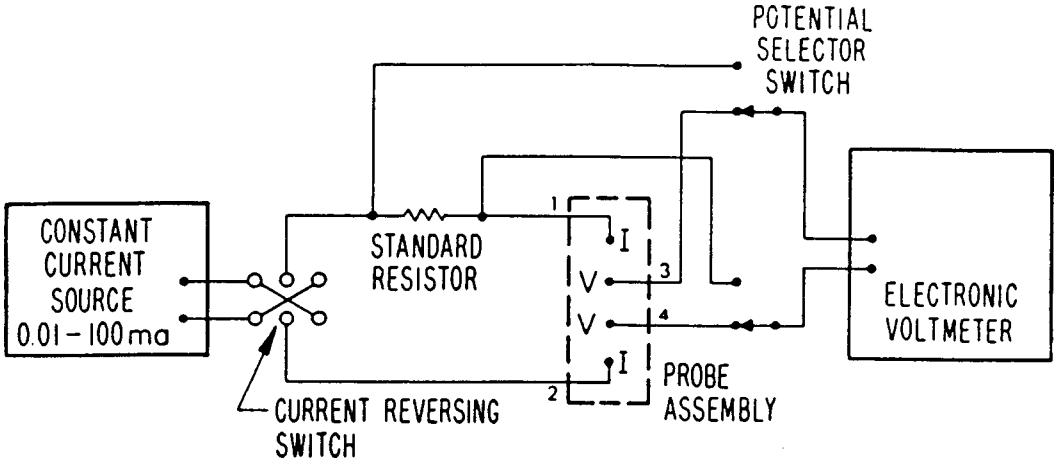


FIG. 1 Schematic of Measurement Circuit Showing Use of a Standard Resistor and a Probe Wired for Configuration A

silicon substrates, it will generally be necessary to accept measurements with fewer significant figures or else to use a current supply with an output above the common maximum of 100 mA, or else to use a voltmeter with submicrovolt resolution.

7.5.1.2 *Standard Resistor*, used to monitor the value of the measurement current if the current supply does not meet the accuracy of settability given in 7.5.1.1. The standard resistor shall be selected to give a potential difference of 0.5 to 5 times that measured across the specimen. This requires the standard resistor to have a value from 2.5 to 25 times the sheet resistance of the layer. The value of the standard resistor must be known at least to four significant digits.

7.5.1.3 *Switches—Double Pole*, double throw switch for reversing the direction of the current, and four pole, double throw switch for changing the probe configuration. The switching functions may be accomplished by wafer switches or relays. Isolation between all switch poles or relays must be 10^6 times the sheet resistance of the layer being measured; isolation of $10^9\Omega$, or greater is recommended.

7.5.1.4 *Electronic Voltmeter*—To read the potential difference across the specimen and standard resistor, or if calibrated in conjunction with the current source, to read the voltage-current ratio directly. The voltmeter shall be capable of measuring d-c voltages between 1 and 100 mV full scale, and be able to resolve the measured voltages to 0.01 %, or better. The meter must have an input impedance of at least $10^9\Omega$.

7.5.2 *Analog Test Circuit*—Five resistors connected as shown in Fig. 2 shall be used according to the procedure of 11.3 for evaluating the accuracy and precision of the electronics in the presence of large series resistors simulating the probe contact resistances. Several circuits of this type may be needed with the resistance of the central resistor, r, of each being, selected according to the expected sheet resistance of the layer to be measured, as listed in Table 2.

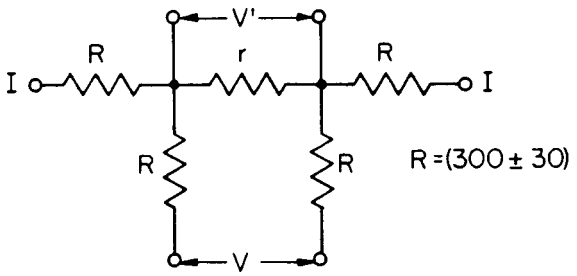


FIG. 2 Analog Test Circuit, Simulating the Contact Resistances in a Four-Probe Measurement

7.5.3 *Conductivity-Type Instrument*—Apparatus in accordance with Method A of Test Methods F 42.

7.6 *Computer Control*— It is intended that this test method will be under control of a computer for positioning the sample at each of the intended measurement sites, lowering the probes, and performing all necessary control of circuit switching, setting of current values, and measuring and logging voltages. It is beyond the scope of this test method to specify details of the computer-based automation.

8. Reagents and Materials

8.1 *Purity of Reagents*—All chemicals for which such specifications exist shall conform to SEMI specifications C1. Other grades may be used, provided it is first determined that the chemical is of sufficiently high purity to permit its use without lessening the accuracy of the test.

8.2 *Purity of Water*— Reference to water shall be understood to mean deionized water (DI) meeting the resistivity and impurity specifications of Type I reagent water in Specifications D 1193.

8.3 *Qualification Wafers*:

8.3.1 *Polished Silicon Wafers*, of any convenient diameter for making probe impressions to be inspected for general probe related damage and contact size and shape. It is useful to divide the surface into rectangular regions by use of scribe lines or

TABLE 2 Nominal Values of the Standard Resistor and of the Center-Leg Resistor, r, for the Analog Circuit Appropriate to Various Sheet Resistance Ranges

Sheet Resistance, Ω	Analog and Standard Resistor, Ω [A]
<2.5	1
2–25	10
20–250	100
200–2500	1000
2000–25 000	10 000

[A] The resistance shall be within a range from one-half to twice the value listed and its value shall be known to 0.05 %.

similar technique to aid in locating a particular series of impressions under the inspection microscope.

8.3.2 One, or more, wafers from each of the processes to be evaluated, for testing the electrical suitability of a given probe for the intended evaluation.

8.4 *Reagents for Surface Treatment*—If surface treatment is required, the following chemicals may be needed:

8.4.1 *Buffered HF*, 10:1 or more dilute,

8.4.2 *Oxidizing Cleaning Solution*, such as that called pirahna clean, which consists of the following:

8.4.2.1 *Concentrated Sulfuric Acid*, 98 wt %

8.4.2.2 *Hydrogen Peroxide*, 30 wt % and

8.4.2.3 *DI Water*.

9. Sampling

9.1 In the case of referee measurements, it is left to the parties to the test to agree upon the number of wafers from a batch, and their selection procedure, as well as the number and location of test positions on each wafer.

9.2 In the case of nonreferee measurements, for example, process control or research applications, it is left to the user of this test to determine the number and location of test positions on each wafer.

10. Suitability of Test Specimen

10.1 The front and back surfaces of the wafer to be measured should be tested for conductivity type using Method A of Test Methods F 42. If they are of the same conductivity type, a thin sheet of insulating material, such as mica, should be placed between the wafer and the stage. This test is not necessary if the front and back surfaces are known to be of opposite conductivity type or if the layer is fully isolated from the substrate by a dielectric layer.

10.2 If the wafer to be measured was fabricated by a process that uses“ finger” clamps or other types of clamping that intrude into the top surface area of the water, the wafer is unsuitable for use with sampling plans that require measurements within several probe spacings from the wafer perimeter.

11. Preparation of Apparatus

11.1 *Visual Inspection of Probe Impressions*—This inspection should be performed when a new, rebuilt or reconditioned probe is first installed to get an initial indication of the mechanical performance of the probes. Once a probe is installed, meets the visual inspection criteria, and is left mounted, visual inspection of probe impressions is generally not needed; functional probe performance tests detailed in 11.2 generally suffice to qualify the probe for continued use. Further visual inspection of probe impressions is advised, however, when a probe has trouble meeting the requirements of 11.2.1. More routine inspection of probe impressions is also advised if probes are interchanged routinely for special applications, thus increasing the risk of changes in the alignment or rigidity of the probe mounting.

11.1.1 After selecting a probe for the intended application, make a series of at least 10 probe impressions on a polished silicon surface in steps of 50 to 125 µm (0.002 to 0.005 in.). Examine the impressions from each of the pins to determine that there is no probe skidding, no cracks or fracture lines surrounding any of the impressions, and that the impressions are generally compact in nature (see Fig. 3).

11.1.2 If fracture lines are seen, the probe must be replaced, or conditioned on surfaces of ceramic, sapphire, lapped silicon or other suitable, non-contaminating material until sets of impressions can be made that do not exhibit fracture. After a conditioning process, it is useful to clean the probe tips with methanol on a cotton swab to loosen debris that may have collected in the tip.

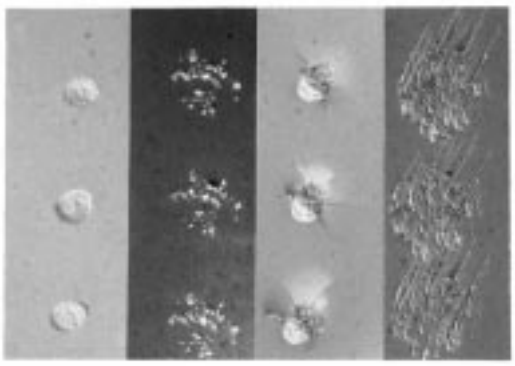
11.1.3 If probe skidding is seen, tighten or otherwise adjust the probe clamp and probe lowering mechanism to eliminate skidding.

11.1.4 If non-compact probe impressions are seen, acceptable data may result, but the probe tip(s) are generally in an advanced state of wear and may not be stable with use.

11.2 *Probe Performance Verification*—This test must be performed before any series of referee measurements, or if a type of layer is being measured for which there is not past experience regarding proper selection of probe radius, load and conditioning. It qualifies a probe for taking highly repeatable measurements, as are needed for mapping spatial variations of sheet resistance, but does not ensure accuracy of measured value. It should be performed separately for each type of layer to be measured.

11.2.1 Select a wafer of the type to be checked for uniformity. At five different locations that are reasonably well separated on the wafer, make a series of 10 measurements following the procedure of 12.4, 12.5 to 12.6 and 13.1 and 13.2, using steps no larger than 100 µm between each of the 10 measurement positions. Calculate the average and standard deviation for each of the five sets of measurements. For a probe to be satisfactory for use in measuring layers of this type, the standard deviation must be no more than 0.1 % of the average for at least four of these sets.

11.3 *Qualification of Measurement Electronics*—The suitability and accuracy of the measurement electronics shall be verified immediately prior to a referee measurement unless the equipment is separately demonstrated to be under statistical



NOTE 1—All probe impressions were made with steps of about 50 µm between impressions, and using probes loaded more heavily than would normally be done for measuring thin films; this was done to provide better photographic detail.

FIG. 3 Photographs of Three Indentations Each from (a) a Satisfactory Probe Tip, (b) a Badly Worn Probe Tip, (c) a Probe Tip Causing Conchoidal Fracture, (d) a Probe Tip Showing Skidding

control for measurements of that process. For non-referee applications, use of the analog circuits is helpful for trouble-shooting or performance monitoring of the electronics.

11.3.1 *Analog Test Circuit*:

11.3.1.1 With the current supply short-circuited or turned off, attach the current leads from the analog test circuit of the appropriate resistance value to the current supply and connect the potential leads designated V (see Fig. 2) from the analog circuit to the input of the voltage measuring instrumentation. Allow sufficient time for the electronics to warm up in accordance with the manufacturers instructions.

NOTE 8—**Caution:** Constant-current power supplies often operate at output voltages of several hundred volts when not connected to a load. Any changes of connection to a constant-current supply should be made either with the current supply turned off or with its output short-circuited.

11.3.2 With the current initially in either direction (to be called "forward") adjust its value to give a measured voltage of between 7 and 12 mV (see Table 1 for nominal values). Record the current, I_f, through the analog box, or measure the potential, V_{sf}, across the appropriate standard resistor connected in series with the analog box. Measure the potential, V_{af}, across the analog box. Reverse the direction of the current and record the current, I_r, or measure the potential V_{sr}, across the standard resistor; measure the potential, V_{ar}, across the analog box. Repeat this procedure until ten sets of data have been taken. All values measured and recorded must be known to at least four significant figures.

11.3.3 *Calculations for the Analog Test Circuit*:

11.3.3.1 Calculate the resistance of the analog box resistor for both forward and reverse directions of current using the appropriate form of the equations according to whether, or not, a standard resistor was used as follows:

$$r_f = V_{af} \times R_s/V_{sf} = V_{af}/I_{af} \quad (1)$$

and

$$r_r = V_{ar} \times R_s/V_{sr} = V_{ar}/I_{ar}$$

where:

r_f and r_r = the calculated values for the analog box resistor, with current in the forward and reverse directions, respectively,

R_s = the value of the standard resistor, Ω,

V_{af} and V_{ar} = the potentials measured across the analog box in the forward and reverse directions, respectively,

I_{af} and I_{ar} = the values of the current in the forward and reverse directions, and

V_{sf} and V_{sr} = the potentials measured across the standard resistor in the forward and reverse directions.

11.3.3.2 For each of the ten pairs, r_f and r_r, calculate the average, r_m

$$r_m = ½(r_f + r_r) \quad (2)$$

11.3.3.3 Calculate the overall average, $\bar{r}_m$ of these ten values of r_m:

$$\bar{r}_m = {}^1/_{10} \times \sum_{i=1}^{10} r_{mi} \quad (3)$$

where:

r_{mi} = one of the ten values of r_m calculated in 11.3.3.1.

11.3.3.4 Calculate the sample standard deviation, s_a, of the ten values as follows:

$$s_a = \left(\frac{1}{3}\right) \times \left[\sum_{i=1}^{10} \left(r_{mi} - \bar{r}_m\right)^2\right]^{(1/2)} \quad (4)$$

11.3.4 *Requirements for the Analog Test Circuit*—For the electrical equipment to be suitable for referee measurements at the sheet resistance value just simulated, it must meet the following requirements:

11.3.4.1 The value of $\bar{r}_m$ must be within 0.25 % of the known value of the resistor, r, and

11.3.4.2 The value of the standard deviation, s_a must be no greater than 0.1 % of $\bar{r}_m$.

NOTE 9—If not previously known, the value of the analog circuit resistor may be determined by using the procedure of 11.3.1 to 11.3.3.2 but measuring the potential across the analog box using the connections V′ in Fig. 1.

12. Procedure

12.1 *Specimen Preparation*:

12.1.1 If the specimens have been kept in a clean, non-contaminating atmosphere, or are to be measured within 3 h after fabrication, proceed to 12.2.

12.1.2 Remove possible organic contaminants that may arise from the storage container as follows: Rinse the specimen in acetone for 1 min. Remove. Immediately immerse in isopropyl alcohol for 1 min. Remove. Blow dry with filtered dry nitrogen. Repeat if necessary until specimen is free from visible stains, streaking or other visual evidence of residue.

NOTE 10—The use of hydrofluoric acid is sometimes necessary to remove surface oxide layers, such as implantation screen oxides, prior to measurement. If used, it must be followed by thorough rinsing with DI water to remove acid residues, and the wafer spun or blown dry.

NOTE 11—The use of other solvents for cleaning, and the use of other reagents such as hot mixtures of sulfuric acid and hydrogen peroxide (pirahna), as well as the use of hot-plate cycles, have been reported, and are used in many locations to clean or stabilize samples prior to measurement, particularly in the case of check samples that are retained and tested periodically to qualify the measurement apparatus. The effects of such treatments is being studied by Committee F-1. Until these studies are completed, no recommendations for, or against, their use is made here.

12.2 *Mounting and Checking the Wafer*:

12.2.1 Using vacuum paddle or tweezers, mount the wafer on the stage, so that the wafer center is within 1 mm of the stage center. Clamp the wafer to the stage with vacuum or other means. Lower the probes onto the wafer. If not known measure the electrical resistance between any of the probe pins and the stage to verify that the electrical isolation is at least 10^9 Ω.

12.2.2 Allow sufficient time for the wafer's temperature to equilibrate with that of the stage. Thirty seconds is sufficient if the wafer had been held at room temperature prior to mounting.

Longer times will be necessary if the wafer was recently removed from a reactor or other elevated temperature process.

NOTE 12—The absolute value of the wafer temperature during measurement will affect the absolute values of sheet resistance, particularly for lightly doped layers, but it should not affect the measurement of uniformity of sheet resistance values, as long as the temperature is constant within 0.2°C during measurement of any wafer. However, the referee measurements, or process control applications where the absolute sheet resistance values are likely to be an important part of the measurement results, it is important to try to maintain the stage temperature within a narrow range for all usage, for example, 23 ± 1°C, or to develop an empirical relation between sheet resistance and measurement temperature for each layer fabrication process of interest.

12.3 *Measurement Site Selection*—Using the measurement site selection agreed to for a referee measurement or that decided upon for process control or other application, follow 12.4 through 12.6 at each measurement site before raising the probe and moving to the next site.

NOTE 13—Various site selection plans may be chosen according to the application needs. These include, but are not limited to: diameter scans with step sizes appropriate to the spatial resolution needed, sparse sampling extensions of the 5-point and 9-point plans described in Test Method F 81, and areal sampling plans with the size of the area and number of points chosen by measurement time constraints and process information requirements. This test method makes no recommendation about choice of sampling plans, since user needs and interests are widely varied. A very useful equal-area measurement plan has been described that can be tailored to many applications **(6)**.

NOTE 14—If wafer diameter scans are chosen, the probe should not be oriented so that the pins lie exactly along the diameter being scanned. Doing so would risk noisy measurements if probes were placed in previous measurement locations. This may be avoided by slightly misaligning the probe pins with respect to the diameter.

12.4 *Measuring in Configuration A to Obtain* R_a—Connect the probe to the electronics so that the current will flow through the outer pins (designated Pins 1 and 4), and that the specimen voltage will be measured by the digital voltmeter (DVM) using the inner pins (Pins 2 and 3), Fig. 4. Lower the probe into the wafer. Start with the current in either direction (called" forward"), and adjust the current to obtain a specimen voltage between 7 and 12 mV, inclusive. It is recommended that the current value be increased from low levels until the required voltage is obtained, rather than lowering the current from large values. Measure the current (using the proper standard resistor, or by monitoring the set point of a calibrated current supply), and the specimen voltage, each to a resolution of at least 0.01 % of the value. Record the current reading as I_f (14), and the voltage reading as V_f(23). Reverse the direction of the current and again measure the specimen voltage and current to the same resolution. Record the current readings as I_r (14) and the voltage reading as V_r (23). The subscripts used for current and voltage are those of the pins that perform the current-carrying and voltage-measuring functions (see **Caution**, Note 8).

12.5 *Measuring in Configuration B to Obtain* R_b—Without raising the probe from the measurement site, connect the probe to the current supply so the current flows through one of the outer probes, and the nonadjacent inner probe, Fig. 5. (There are two ways of doing this that should provide equivalent results.) Connect the remaining two probes to the voltmeter,

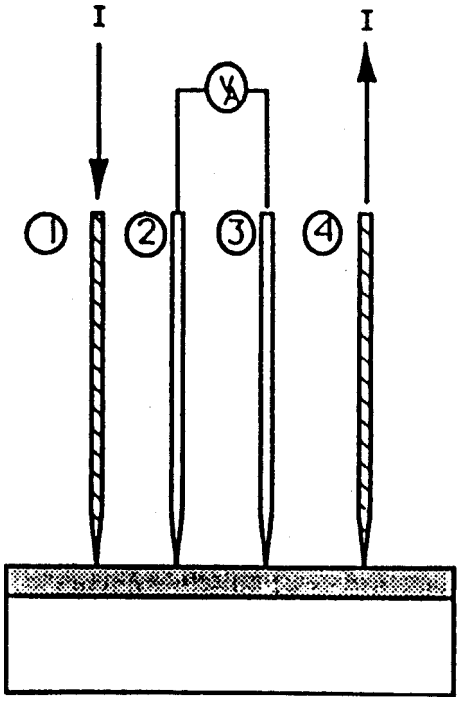
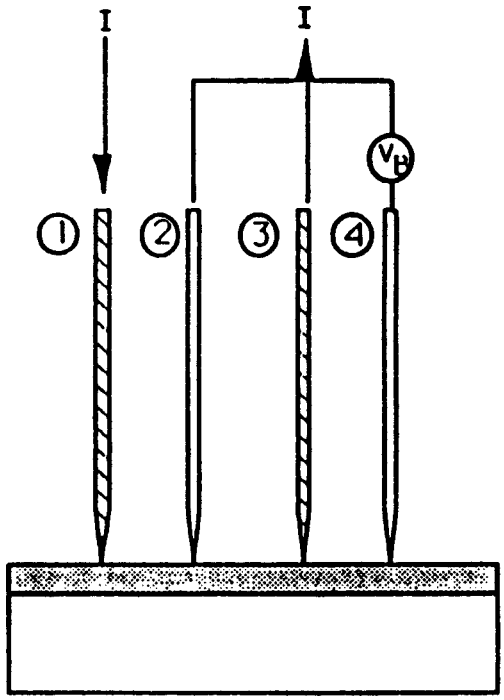


FIG. 4 Schematic Wiring of Four-Point Probe for Measurement in Traditional Configuration A



NOTE 1—Interchanging the roles of current and voltage probes gives the other choice.

FIG. 5 Schematic Wiring of Four-Point Probe in One of the Two Choices for Configuration B

making sure that the wiring polarity corresponds to that used for the connections to the current supply. With the current in the forward direction, measure and record the current as I_f (13) and the voltage as V_f (24), with the same resolution as in 12.4.1. Reverse the direction of the current; measure and

record the current I_r (13) and the voltage as V_r (24).

NOTE 15—The notation in 12.5.1 assumes Pins 1 and 3 were used for current, and Pins 2 and 4 were used for specimen voltage measurement. If the other choice of wiring the probe for Configuration *B* were used, the subscript notation in 13.5.1 would be changed accordingly.

12.6 *Moving to the Next Measurement Site*:

12.6.1 Turn off, or short circuit, the output of the current supply; raise the probe and move the stage to the next measurement site. Follow the procedure of 12.4 and 12.5 at this and all other sites.

12.6.2 The current at each measurement site may be kept at the value used for the first site, or it may be readjusted for each site to give a specimen voltage across the specimen sites that is within very tight limits. Whenever the probes are lowered or the current is changed, make sure that there is a short pause to ensure that the probes, the current supply, and the measurement voltage lines have stabilized before taking data. Depending on the wafer type and the design of the instrumentation, this may be from a fraction of a second to several seconds.

12.6.3 Measure and record the temperature of the stage to the nearest 0.1°C at least at the beginning and the end of the measurements. Actual measurement of temperature for each measurement site is preferred if experience indicates that noticeably drift or fluctuation (greater than 1°C) is likely to occur during the course of the measurements.

13. Calculations

13.1 *Calculation of R_a and R_b for Each Site*:

13.1.1 Calculate the average of the forward voltage-current ratio and the reverse voltage-current ratio as follows to obtain R_a:

$$R_a = ½[V_f(23) / I_f(14) + V_r(23) / I_r(14)] \quad (5)$$

where:

R_a = the resistance from Configuration *A*.

13.1.2 Calculate the average of the forward voltage-current ratio and the reverse voltage-current ratio as follows to obtain R_b:

$$R_b = ½[V_f(24) / I_f(13) + V_r(24) / I_r(13)] \quad (6)$$

where:

R_b = the resistance from Configuration B.

13.1.3 The forward and reverse voltage-current ratios must agree within 5 % of the larger of these ratios both for R_a and for R_b in order to be acceptable for use in referee measurements.

13.2 *Calculation of the Sheet Resistance at Each Site* **(2)**—For each measurement site, calculate the sheet resistance, R_s, as follows:

$$R_s = K_a R_a \quad (7)$$

where:

$$K_a = -14.696 + 25.173(R_a/R_b) - 7.872(R_a / R_b)^2 \quad (8)$$

13.3 *Reviewing the Data*—Many applications of uniformity testing involve acquisition of large amounts of data. It is generally beneficial to review these data before interpreting them simply as manifestations of sheet resistance nonuniformity. A useful technique is to plot the values obtained for R_s as a time sequence, that is, in the order the data for the site were taken for these sides. Examination of this plot may be correlated with measurement site coordinates to reveal unexpected edge proximity effects or regions of the wafer that have unusual nonuniformity that may need to be reprobed with a different site-selection plan. Examination may also reveal one or more points that are highly inconsistent with adjacent points possibly indicating problems due to vibrations or spots of surface contamination. Note such observations, but do not delete or edit the data, unless agreed upon by all parties to the test.

13.4 *Analysis and Summary of Data*—The sheet resistance data may be analyzed and summarized in a number of ways as agreed upon by parties to referee test, or as appropriate for process control or other applications. These may include, but are not limited to: listing of all data with site coordinates, contour plots of the deviations from average value, and distributional statistics of the data.

14. Report

14.1 The report shall include the following information:

14.1.1 Operator's name, date and time of measurements,

14.1.2 Wafer identification number and description,

14.1.3 Identification of instrument used, by manufacturer, serial number, and model number,

14.1.4 Identification of probe used, by manufacturer, serial number and probe spacing, probe tip radius and material, and probe force specifications,

14.1.5 Statement of site location plan used,

14.1.6 Initial and final temperature at wafer stage for the measurement sequence,

14.1.7 Summary of sheet resistance data as chosen in connection with 13.4.1,

14.1.8 Notations about aberrant measurement sites as identified by any data screening procedures employed, and

14.1.9 Data from probe qualification tests.

15. Precision and Bias

15.1 *Precision*—Multilaboratory tests to evaluate the precision of sheet resistance uniformity measurements are being conducted on a variety of wafers types by Subcommittee F01.95. A specified measurement site plan using 81 measurement sites is being employed by all participants. The standard deviation of values for the 81 sites will be used to compute the multilaboratory precision.

15.1.1 A straightforward propagation of errors based on the performance specifications, in order to estimate the precision, does not appear possible. Required instrument resolution, power supply stability, and probe performance qualification are designed to allow a relative accuracy and precision of better than 0.1 % for all measurement sites on a wafer. However, for wafers with high uniformity (for example, standard deviation of all measurement site values on the order of 0.2 %), even these requirements may not ensure good two-party, or multilaboratory agreement on the wafer uniformity.

15.1.2 Single laboratory values for reproducibility of the measurement of wafer uniformity are obtained from tests run by Subcommittee F1.95 in 1991. For those tests, five types of wafers with average sheet resistance values from about 15 Ω to

about 400 Ω were tested, as detailed in Annex A1. In those tests, a standard deviation, (in percent), was used to represent the uniformity values obtained for each of the wafers. While it is common to give reproducibility values as a standard deviation, in order to avoid confusion from duplication of terminology, the reproducibility of the repeated determinations of nonuniformity for each type wafer will be given here as the range of standard deviation values obtained in the original tests.

15.1.2.1 Range of uniformity values obtained, organized by nominal sheet resistance of the wafer being tested:

14.5 Ω — 0.24 % to 0.24 %
144 Ω — 0.81 % to 0.86 %
4000 Ω — 1.53 % to 1.62 %.
26 Ω— 0.67 % to 0.69 %
570 Ω— 1.83 % to 1.89 %

15.2 These wafers in these tests were fabricated by five different processes. The purpose of these tests is to demonstrate the consistency of determination of sheet resistance uniformity with dual-configuration four-probe measurements, not to determine the uniformity achievable by a given process. The five processes utilized are capable of both better and poorer uniformity than seen here. The reproducibility of uniformity values given here represent good measurement practice but the consistency of values for each wafer might have been even better if all measurements had been taken over a shorter time interval.

15.3 *Bias*—A statement of bias cannot be made because there are no semiconductor reference artifacts with a known level of nonuniformity.

16. Keywords

16.1 epitaxy; four-point probe; ion implant; metallization; polysilicon; sheet resistance; silicon

ANNEX

(Mandatory Information)

A1. SINGLE LAB TEST RESULTS

A1.1 One wafer from each of five different thin film types was tested for uniformity. Each was 100-mm diameter. A measurement test-site plan using 81 test locations located at wafer center and on four equally spaced circles with a maximum radius of 38.1 mm was used for all measurements. The measure of uniformity for measurements on each wafer was the standard deviation of the 81 measured values expressed as a percent of the mean measured value. For each of the wafers, 11 to 13 tests of uniformity were run over periods that ran from 3 to 6 months, depending on the individual wafer.

A1.1.1 Temperatures of the wafer stage were monitored and recorded. Average sheet resistances were found to change as a function of temperature but no corresponding corrections of sheet resistance values were made because the temperature coefficients of resistivity were not known for the films involved. The assumption was made that the determination of uniformity should be minimally affected as long as the temperature stayed relatively constant during the course of each measurement run. Results of this test are summarized in Table A1.1. The highest temperatures used for each wafer were achieved by deliberate elevation of room temperature in order to determine whether temperature affected average sheet resistance or uniformity value. Temperature dependence of average sheet resistance was seen for wafer Types 1, 2 and 5. No dependence of sheet resistance uniformity on temperature was seen.

A1.2 An additional test involved three measurements of uniformity on each of three different wafers from the same five thin-film fabrication processes. These tests were completed within three days. They were also associated with evaluation of the repeatability capability of the sheet resistance measurement instrumentation. For this evaluation of the instrument, 50 measurements were made on each wafer by taking 10 very closely spaced measurements in each of five relatively widely separated locations on the wafer. The assumption was made that in each group of ten, the measurements were so closely spaced compared to the sampling volume of the four-point

TABLE A1.1 Summary of Sheet Resistance Uniformity Tests Made by Dual-Configuration Four-Point Probe Measurements at One Laboratory on One Wafer from Each of Five Thin Film Fabrication Processes

Process	Nominal Resistance, Ω	Number of Test Runs	Range of Temperatures, C	Range of Mean Values, [A] Ω	Range of Uniformity Values, %
(*1*) Boron Implant 1.3×10^{13}/60 keV	570	13	19.35–28.45	566.3–574.6	1.83–1.89
(*2*) Phosphorus Implant 5×10^{14}/100 keV	144	13	20.21–27.73	143.4–144.4	0.81–0.86
(*3*) Arsenic Implant 5×10^{15}/60 keV	26	13	20.94–32.48	26.33–26.78	0.67–0.69
(*4*) Polysilicon 600-nm thickness 900° deposition temperature	14.5	11	21.41–26.00	14.48–14.55	0.24–0.24
(*5*) N/P-epitaxy 3 µm/1.2 Ω cm	4000	11	20.23–30.92	4021–4301	1.53–1.62

[A] Measurements were not corrected for changes in temperature.

probe that any variability experienced was a measure of the equipment repeatability (imprecision) and was not caused by variations in the thin film itself. The actual measurements of wafer uniformity used the same 81-point test pattern as used for the wafers in A1.1.

A1.2.1 The measurements from this test, summarized in Table A1.2, show that for each process, the three wafers have a different average sheet resistance, even when measured at the same nominal temperature and they also have rather different levels of nonuniformity as determined from the standard deviations of the 81 measurements. The variations of these run-to-run standard deviations for a given wafer is seen to be small compared to the typical wafer-to-wafer standard deviations for the different wafers from a given process.

A1.2.2 While not shown here, the contour maps that were developed from the uniformity data clearly show different patterns or fingerprints for the individual wafers. These contour map patterns were very reproducible from run to run.

TABLE A1.2 Uniformity Results from 3 Runs on 3 Waters Each from 5 Different Processes

Process	Instrument Precision, %	Wafer Parameter[A]	Round 1	Round 2	Round 3
Boron Implant	0.028	Average Resistance	534.8	531.8	534.1
Wafer 4		Standard Deviation	0.69 %	0.68 %	0.74 %
		Temperature Range	26.0–26.2°C	19.4–20.1°C	23.4–23.9°C
Boron Implant	0.028	Average Resistance	556.4	553.8	554.7
Wafer 5		Standard Deviation	1.23 %	1.22 %	1.23 %
		Temperature Range	25.6–25.9°C	20.4–21.1°C	24.2–24.7°C
Boron Implant	0.028	Average Resistance	550.7	547.8	549.7
Wafer 6		Standard Deviation	1.35 %	1.34 %	1.33 %
		Temperature Range	25.6–26.0°C	21.0–21.6°C	24.6–25.0°C
Phos. Implant	0.18	Average Resistance	147.5	148.1	147.5
Wafer 4		Standard Deviation	0.71 %	0.71 %	0.69 %
		Temperature Range	20.4–21.0°C	24.9–25.2°C	20.5–21.2°C
Phos. Implant	0.018	Average Resistance	149.4	149.7	149.2
Wafer 5		Standard Deviation	0.81 %	0.81 %	0.82 %
		Temperature Range	21.4–21.9°C	24.9–25.2°C	21.6–22.3°C
Phos. Implant	0.018	Average Resistance	145.9	146.0	146.0
Wafer 6		Standard Deviation	1.45 %	1.45 %	1.45 %
		Temperature Range	22.4–22.8°C	22.1–22.7°C	22.4–22.9°C
As Implant	0.012	Average Resistance	26.16	26.16	26.16
Wafer 4		Standard Deviation	0.57 %	0.56 %	0.56 %
		Temperature Range	22.7–23.2°C	21.5–22.0°C	22.8–23.4°C
As Implant	0.012	Average Resistance	25.06	24.88	24.93
Wafer 5		Standard Deviation	0.77 %	0.77 %	0.77 %
		Temperature Range	22.0–27.0°C	22.2–22.7°C	23.4–24.0°C
As Implant	0.012	Average Resistance	27.55	27.34	27.44
Wafer 6		Standard Deviation	0.74 %	0.74 %	0.74 %
		Temperature Range	26.6–26.7°C	22.8–23.3°C	263.9–24.5°C
Polysilicon	0.009	Average Resistance	15.88	15.86	15.84
Wafer 4		Standard Deviation	0.59 %	0.58 %	0.59 %
		Temperature Range	24.2–24.7°C	23.0–23.5°C	22.1–22.6°C
Polysilicon	0.009	Average Resistance	14.69	14.72	14.69
Wafer 5		Standard Deviation	0.29 %	0.29 %	0.29 %
		Temperature Range	24.6–25.0°C	23.5–24.0°C	22.1–22.6°C
Polysilicon	0.009	Average Resistance	16.97	16.96	16.93
Wafer 6		Standard Deviation	0.32 %	0.31 %	0.32 %
		Temperature Range	24.9–25.3°C	23.8–24.3°C	22.2–22.7°C
N/P epitaxy	0.08	Average Resistance	3982	3933	3961
Wafer 4		Standard Deviation	0.89 %	0.73 %	0.69 %
		Temperature Range	23.6–23.7°C	20.4–21.0°C	21.4–22.0°C
N/P-epitaxy	0.08	Average Resistance	3857	3800	3805
Wafer 5		Standard Deviation	1.58 %	1.60 %	1.56 %
		Temperature Range	23.6–24.0°C	21.5–22.1°C	21.4–22.0°C
N/P-epitaxy	0.08	Averager Resistance	3929	4006	3940
Wafer 6		Standard Deviation	1.66 %	1.75 %	1.67 %
		Temperature Range	19.5–20.0°C	22.4–22.9°C	20.7–21.3°C

[A] The temperature range given is variation within each individual measurement run of 81 test sites. In Table A1.1 the temperature range given is the variation of the average temperature for each of the test runs.

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